Refine Search

Search Results -

Terms	Documents
L1 and bus	33

Database:
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Search: L4

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DATE: Friday, March 19, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L4	L1 and bus	33	L4
L3	L1 and bus and backplane	1	L3
L2	L1 and (bus same backplane)	0	L2
L1	(switch$3 near3 path) same (enabl$3 or disabl$3) same controller same (memory or storage)	44	L1

END OF SEARCH HISTORY

h e b b cg b e e ch

Refine Search

Search Results -

Terms	Documents
L4	0

Database:
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JPO Abstracts Database
Derwent World Patents Index
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Search: L5

Refine Search

Recall Text Clear Interrupt

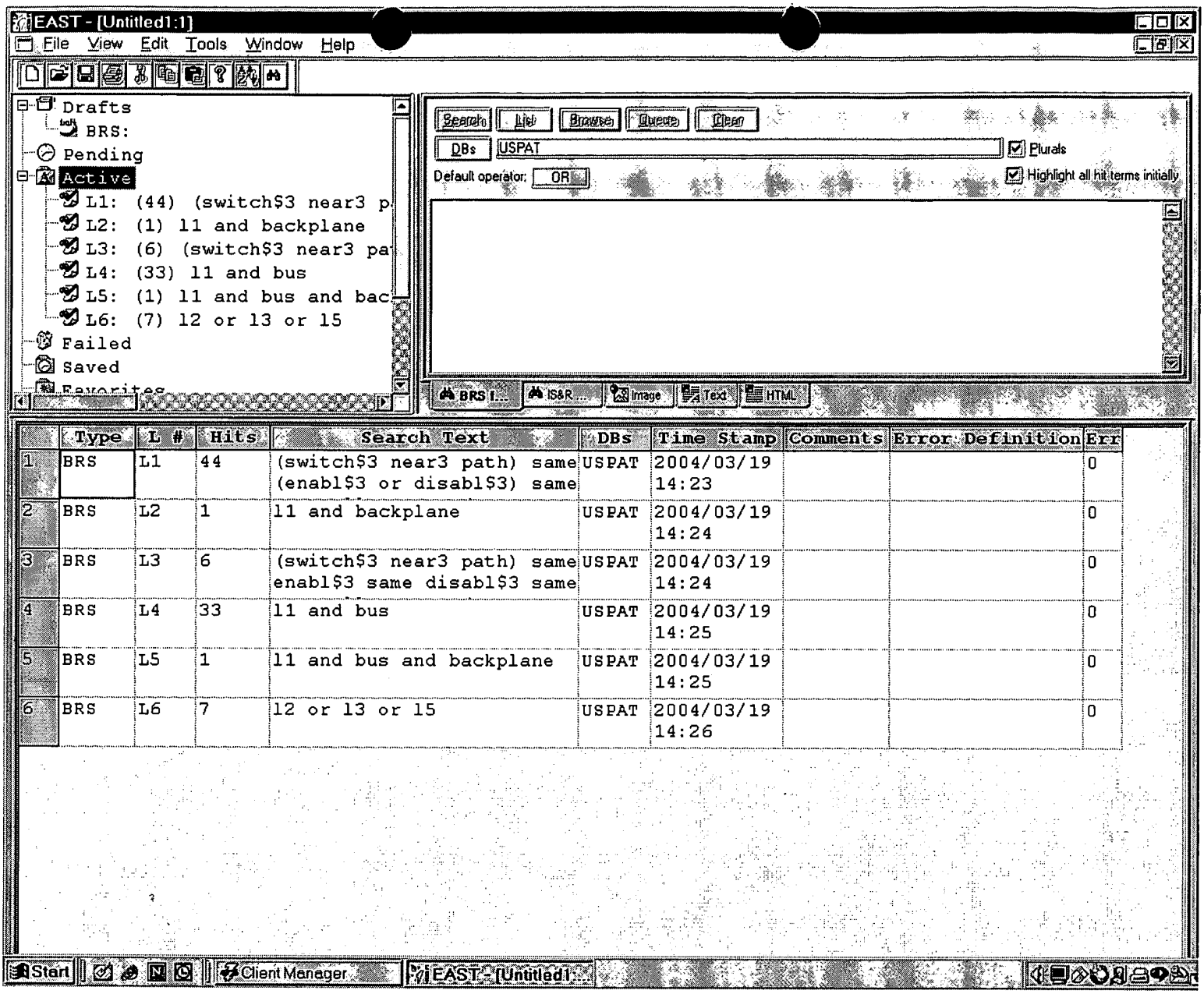
Search History

DATE: Friday, March 19, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L5	L4	0	L5
DB=USPT; PLUR=YES; OP=OR			
L4	L1 and bus	33	L4
L3	L1 and bus and backplane	1	L3
L2	L1 and (bus same backplane)	0	L2
L1	(switch$3 near3 path) same (enabl$3 or disabl$3) same controller same (memory or storage)	44	L1

END OF SEARCH HISTORY

h e b b cg b e e ch



	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
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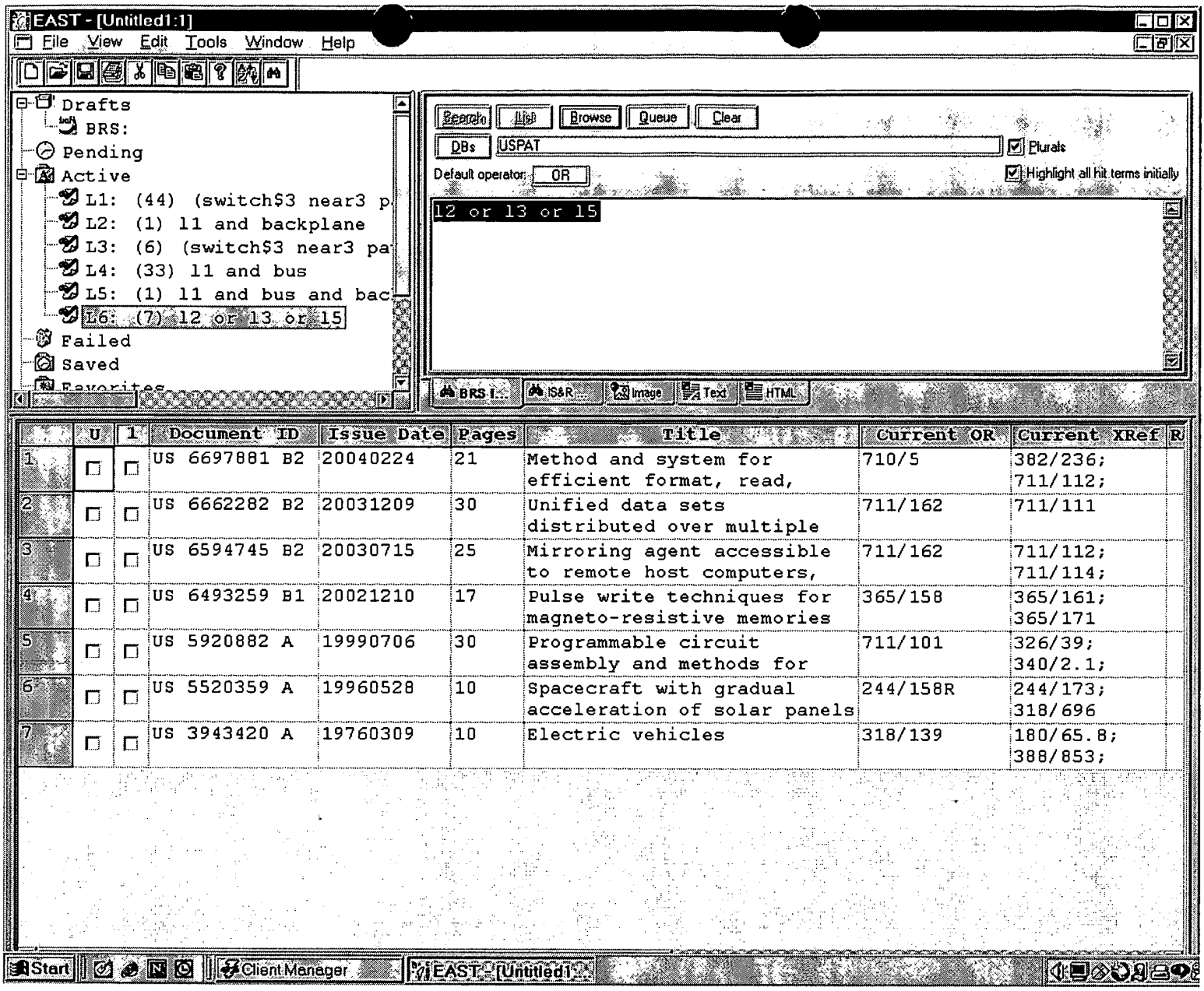
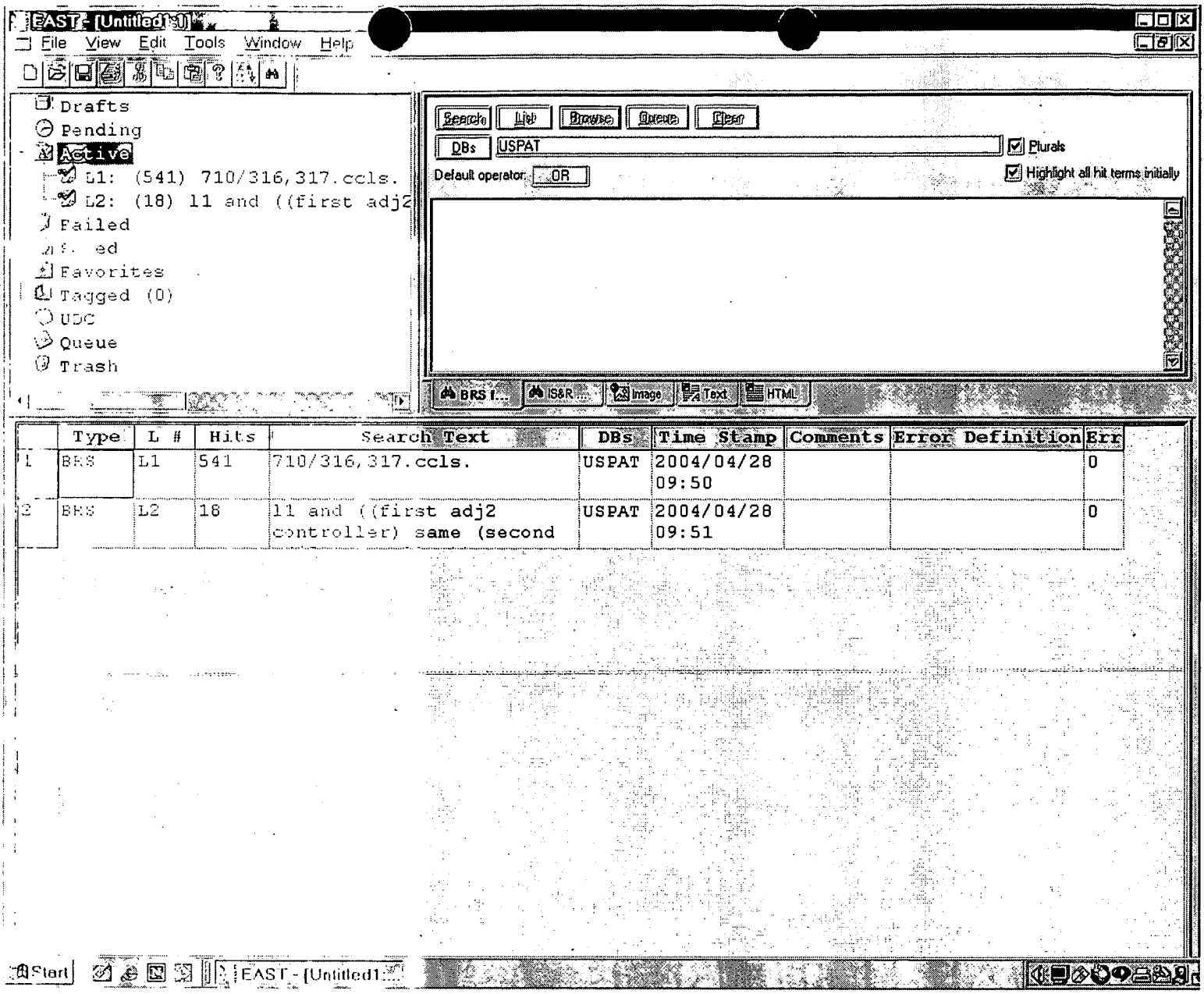
2	BRS	L2	1	l1 and backplane	USPAT	2004/03/19 14:24			0
3	BRS	L3	6	(switch$3 near3 path) same enabl$3 same disabl$3 same	USPAT	2004/03/19 14:24			0
4	BRS	L4	33	l1 and bus	USPAT	2004/03/19 14:25			0
5	BRS	L5	1	l1 and bus and backplane	USPAT	2004/03/19 14:25			0
6	BRS	L6	7	l2 or l3 or l5	USPAT	2004/03/19 14:26			0



	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 6697881 B2	20040224	21	Method and system for efficient format, read,	710/5	382/236; 711/112;	
2	☐	☐	US 6662282 B2	20031209	30	Unified data sets distributed over multiple	711/162	711/111	
3	☐	☐	US 6594745 B2	20030715	25	Mirroring agent accessible to remote host computers,	711/162	711/112; 711/114;	
4	☐	☐	US 6493259 B1	20021210	17	Pulse write techniques for magneto-resistive memories	365/158	365/161; 365/171	
5	☐	☐	US 5920882 A	19990706	30	Programmable circuit assembly and methods for	711/101	326/39; 340/2.1;	
6	☐	☐	US 5520359 A	19960528	10	Spacecraft with gradual acceleration of solar panels	244/158R	244/173; 318/696	
7	☐	☐	US 3943420 A	19760309	10	Electric vehicles	318/139	180/65.8; 388/853;	


EAST - [Untitled1]
File View Edit Tools Window Help
Drafts
Pending
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L1: (541) 710/316,317.ccls.
L2: (18) l1 and ((first adj2
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1 BRS L1 541 710/316,317.ccls. USPAT 2004/04/28 09:50 0
2 BRS L2 18 l1 and ((first adj2 controller) same (second USPAT 2004/04/28 09:51 0
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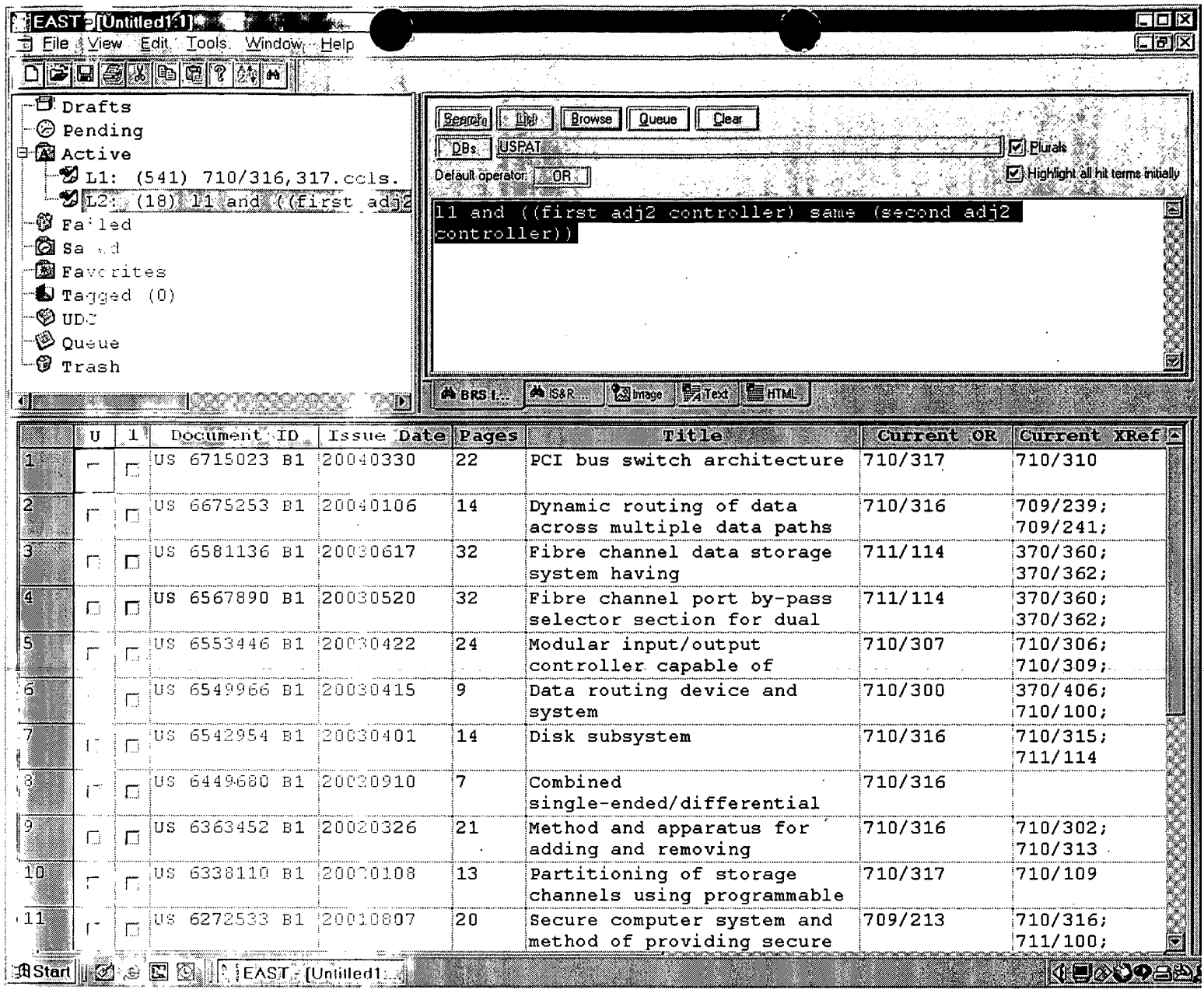
EAST - [Untitled1]



	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6715023 B1	20040330	22	PCI bus switch architecture	710/317	710/310
2	☐	☐	US 6675253 B1	20040106	14	Dynamic routing of data across multiple data paths	710/316	709/239; 709/241;
3	☐	☐	US 6581136 B1	20030617	32	Fibre channel data storage system having	711/114	370/360; 370/362;
4	☐	☐	US 6567890 B1	20030520	32	Fibre channel port by-pass selector section for dual	711/114	370/360; 370/362;
5	☐	☐	US 6553446 B1	20030422	24	Modular input/output controller capable of	710/307	710/306; 710/309;
6		☐	US 6549966 B1	20030415	9	Data routing device and system	710/300	370/406; 710/100;
7	☐	☐	US 6542954 B1	20030401	14	Disk subsystem	710/316	710/315; 711/114
8	☐	☐	US 6449680 B1	20020910	7	Combined single-ended/differential	710/316	
9	☐	☐	US 6363452 B1	20020326	21	Method and apparatus for adding and removing	710/316	710/302; 710/313
10	☐	☐	US 6338110 B1	20020108	13	Partitioning of storage channels using programmable	710/317	710/109
11	☐	☐	US 6272533 B1	20010807	20	Secure computer system and method of providing secure	709/213	710/316; 711/100;

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switch* and path and (enabl* or disabl*)<and>contro Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **A high I/O reconfigurable crossbar switch**
Young, S.; Alfke, P.; Fewer, C.; McMillan, S.; Blodget, B.; Levi, D.;
Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th A IEEE Symposium on , 9-11 April 2003
Pages:3 - 10

[Abstract] [PDF Full-Text (3138 KB)] **IEEE CNF**

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2 **Generalized guaranteed rate scheduling algorithms: a framework**
Goyal, P.; Vin, H.M.;
Networking, IEEE/ACM Transactions on , Volume: 5 , Issue: 4 , Aug. 1997
Pages:561 - 571

[Abstract] [PDF Full-Text (368 KB)] **IEEE JNL**

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3 **Activity-sensitive architectural power analysis**
Landman, P.E.; Rabaey, J.M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 15 , Issue: 6 , June 1996
Pages:571 - 587

[Abstract] [PDF Full-Text (1839 KB)] **IEEE JNL**

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4 **The trajectory tracking approach-a new method for minimum distor PWM in dynamic high-power drives**
Holtz, J.; Beyer, B.;
Industry Applications, IEEE Transactions on , Volume: 30 , Issue: 4 , July-Au 1994
Pages:1048 - 1057

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[Abstract] [PDF Full-Text (752 KB)] **IEEE JNL**

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Activity-sensitive architectural power analysis**
Landman, P.E.; Rabaey, J.M.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 15 , Issue: 6 , June 1996
Pages:571 - 587

[Abstract] [PDF Full-Text (1839 KB)] IEEE JNL

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A high I/O reconfigurable crossbar switch

Young, S. Alfke, P. Fewer, C. McMillan, S. Blodget, B. Levi, D.
Xilinx Inc., Longmont, CO, USA

This paper appears in: **Field-Programmable Custom Computing Machines, 2003. FCCM 2003. 11th Annual IEEE Symposium on**

Publication Date: 9-11 April 2003
On page(s): 3 - 10
ISSN: 1082-3409
Number of Pages: x+312
Inspec Accession Number: 7756113

Abstract:
A crossbar **switch** with 928 inputs and 928 outputs is presented. **Switching** elements are constructed using logic in the routing fabric. This approach yields a 16/spl times/ improvement in logic density compared with using conventional logic. Normally, the routing is fixed. However, in FPGAs (field programmable gate arrays), the interconnection is defined by the state of SRAM configuration cells, which are dynamically modifiable. Therefore, the **switch** is implemented on an FPGA using partial configuration to modify routing resources during operation. All **paths** are synchronously clocked at 155.5 MHz, creating a total throughput of 144.3 Gbits/s. to maintain constant clock latency across all **paths**, partially configurable delay registers are used. Finally, the partial reconfiguration **controller** is implemented in hardware to **enable** fast **switch** updates.

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Index Terms:

field programmable gate arrays logic circuits reconfigurable architectures **switching** circuits FPGA SRAM configuration cell configurable delay register field programmable gate array logic reconfigurable crossbar **switch** reconfiguration **controller** routing resource modification

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Activity-sensitive architectural power analysis

Landman, P.E. Rabaey, J.M.
DSP R&d Center, Texas Instrum. Inc., Dallas, TX, USA;

This paper appears in: **Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on**

Publication Date: June 1996
On page(s): 571 - 587
Volume: 15 , Issue: 6
ISSN: 0278-0070
Reference Cited: 30
CODEN: ITCSDI
Inspec Accession Number: 5311455

Abstract:
Prompted by demands for portability and low-cost packaging, the electronics industry has begun to view power consumption as a critical design criterion. As such there is a growing need for tools that can accurately predict power consumption early in the design process, many high-level power analysis models do not adequately model activity, however, leading to inaccurate results. This paper describes an activity-sensitive power analysis strategy for datapath, memory, control **path**, and interconnect elements. Since datapath and memory modeling has been described in a previous publication, this paper

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focuses mainly on a new Activity-Based Control (ABC) model and on a hierarchical interconnect analysis strategy that **enables** estimates of chip area as well as power consumption. Architecture-level estimates are compared to **switch**-level measurements based on net lists extracted from the layouts of three chips: a digital filter, a global **controller**, and a microprocessor. The average power estimation error is about 9% with a standard deviation of 10%, and the area estimates err on average by 14% with a standard deviation of 6%

Index Terms:

circuit analysis computing integrated circuit interconnections integrated circuit layout integrated circuit modelling SPA tool activity-based control model activity-sensitive architectural power analysis chip area esimation critical design criterion hierarchical interconnect analysis strategy power consumption

Reference list:

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[Abstract] [PDF Full-Text (1088KB)]

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[Abstract] [PDF Full-Text (592KB)]

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[Abstract] [PDF Full-Text (368KB)]

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[Abstract] [PDF Full-Text (460KB)]

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☐ 1. Document ID: US 6651131 B1

L4: Entry 1 of 4 File: USPT Nov 18, 2003

US-PAT-NO: 6651131
DOCUMENT-IDENTIFIER: US 6651131 B1

TITLE: High bandwidth network and storage card

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 2. Document ID: US 6507581 B1

L4: Entry 2 of 4 File: USPT Jan 14, 2003

US-PAT-NO: 6507581
DOCUMENT-IDENTIFIER: US 6507581 B1

TITLE: Dynamic port mode selection for crosspoint switch

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6334164 B1

L4: Entry 3 of 4 File: USPT Dec 25, 2001

US-PAT-NO: 6334164
DOCUMENT-IDENTIFIER: US 6334164 B1

TITLE: Bus system for use with information processing apparatus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 5506973 A

L4: Entry 4 of 4 File: USPT Apr 9, 1996

US-PAT-NO: 5506973
DOCUMENT-IDENTIFIER: US 5506973 A
** See image for Certificate of Correction **

h e b b g e e e f e be ef b e

TITLE: Bus system for use with information processing apparatus

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

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L2: Entry 16 of 16 File: USPT Jun 25, 1996

DOCUMENT-IDENTIFIER: US 5530842 A
TITLE: Generic backplane system which is configurable to serve different network access methods simultaneously

CLAIMS:

4. A communication system concentrator according to claim 1, wherein:

each of said media modules includes port switching means for connecting and disconnecting individual ports to one of said physical circuits of said generic passive backplane element and connecting and disconnecting individual ports to other individual ports and for isolating connected individual ports from said physical circuits of said generic passive backplane element for communication only between connected individual ports, said port switching means including hardware switches controlled by software for creating a logical network topology by selectively connecting and disconnecting ports from said physical paths of said generic passive backplane element.

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L2: Entry 16 of 16 File: USPT Jun 25, 1996

US-PAT-NO: 5530842
DOCUMENT-IDENTIFIER: US 5530842 A

TITLE: Generic backplane system which is configurable to serve different network access methods simultaneously

DATE-ISSUED: June 25, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Abraham; Menachem	Lexington	MA		
Bartolini; David	Dudley	MA		
Ben-Meir; Samuel	Sharon	MA		
Carmi; Ilan	Framingham	MA		
Cook, III; John L.	Southborough	MA		
Hart; Ira	Cambridge	MA		
Herman; Alex	Sharon	MA		
Horowitz; Steven E.	Holliston	MA		
Kim; Yongbum	Brookline	MA		
Linde; Yoseph	Needham	MA		
Ramelson; Brian	Brighton	MA		
Rehberg; Richard	Northboro	MA		
Saussy; Gordon	Brighton	MA		
Shohet; Yuval	Acton	MA		
Zhovnirovski; Igor	Lexington	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
3COM Corporation	Santa Clara	CA			02

APPL-NO: 08/ 221383 [PALM]
DATE FILED: March 31, 1994

PARENT-CASE:
This is a continuation of application Ser. No. 07/687,590 filed Apr. 16, 1991 which is a continuation in part of application Ser. No. 07/512,849 filed on Apr. 23, 1990 now abandoned.

INT-CL: [06] G06 F 9/00, G06 F 15/00

US-CL-ISSUED: 395/500; 395/800, 395/200.1, 395/200.15, 395/200.21, 364/229.4, 364/240.1, 364/242.94, 364/242.95, 364/242.96, 364/DIG.1
US-CL-CURRENT: 709/221; 370/434, 370/445

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FIELD-OF-SEARCH: 395/800, 395/200, 395/500, 395/325, 395/275, 395/725, 395/775, 395/200.01, 395/200.10, 395/200.15, 395/200.21, 364/DIG.1, 364/DIG.2, 370/58.1

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U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4418382	November 1983	Larson et al.	395/200
☐	4660141	April 1987	Ceccon et al.	395/275
☐	4760553	July 1988	Buckley et al.	395/575
☐	4763249	August 1988	Bomba et al.	395/325
☐	4835674	May 1989	Collins et al.	395/275
☐	4845609	July 1989	Lighthart et al.	395/275
☐	4872158	October 1989	Richards	370/58.1
☐	5016162	May 1991	Eipstein et al.	395/775
☐	5115235	May 1992	Oliver	
☐	5265239	November 1993	Adolino	395/500
☐	5283869	February 1994	Adams et al.	395/200
☐	5307463	April 1994	Hyatt et al.	395/275
☐	5349343	September 1994	Oliver	

OTHER PUBLICATIONS

Arnold R. G. et al; "A Hierarchical restructurable multi-microprocessor architecture" IEEE 3rd Annual Symposium on Computer Architecture pp. 40-45. 19-21 Jan. 1976.

ART-UNIT: 232

PRIMARY-EXAMINER: An; Meng-Al

ATTY-AGENT-FIRM: McGlew and Tuttle

ABSTRACT:

A local net area network, or LAN, configuration is provided with a multiple generic LAN channel architecture which can be logically and dynamically changed. The configuration control can be applied to each module of the network and to each port of a module of a LAN hub. The architecture provides multiple LAN protocols to be used simultaneously, as needed, through protocol specific functions. Industry standard protocol such as: token bus, token ring, and fiber distributed data interface (FDDI), can be implemented using the generic channel architecture and its characteristics providing respective network functions. The architecture also provides a digital collision detection method and provides information necessary

for precise network statistics monitoring. The token passing ring architecture provides a logical ring formation within the generic channel. A token passing bus architecture uses modified Ethernet.TM. architecture, and a hub management provides control for the generic multichannel and the LAN management provides protocol dependent network management. The architecture provided allows multiple hub management entities via hub mastership arbitration to provide a unique master for the hub management function.

18 Claims, 42 Drawing figures

L3: Entry 6 of 21 File: USPT Aug 21, 2001

DOCUMENT-IDENTIFIER: US 6278959 B1
TITLE: Method and system for monitoring the performance of a data processing system

Detailed Description Text (33):
Four chips illustrated in the example containing cache include path switch controller chip Q1, path switch controller chip Q2, memory controller chip R1 and memory controller chip R2. Each of the chips Q1, Q2, R1, and R2 also contain token enable logic 72 and token passing logic 73. Specifically, chip Q1 contains L3 cache 78 and chip Q2 contains L3 cache 80. In addition, chip R1 contains L4 cache 86 and memory interface 82 and chip R2 contains L4 cache 88 and memory interface 84. Data on chips Q1, Q2, R1 and R2 may be accessed by multiple processor units in addition to processor 70 illustrated in the example.

First Hit Fwd Refs

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L3: Entry 6 of 21 File: USPT Aug 21, 2001

US-PAT-NO: 6278959
DOCUMENT-IDENTIFIER: US 6278959 B1

TITLE: Method and system for monitoring the performance of a data processing system

DATE-ISSUED: August 21, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Alferness; Merwin Herscher	Rochester	MN		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/ 273184 [PALM]
DATE FILED: March 19, 1999

INT-CL: [07] G06 F 15/00

US-CL-ISSUED: 702/186; 702/186, 702/182, 711/117, 711/118, 711/122, 712/43, 712/201

US-CL-CURRENT: 702/186; 702/182, 711/117, 711/118, 711/122, 712/201, 712/43

FIELD-OF-SEARCH: 702/186, 702/182, 700/169, 700/174, 711/117, 711/118, 711/122

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4814978	March 1989	Dennis	712/201
☐	5483468	January 1996	Chen et al.	702/186
☐	5724599	March 1998	Balmer et al.	712/43
☐	5956744	September 1999	Robertson et al.	711/122
☐	5960461	September 1999	Frank et al.	711/163

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ART-UNIT: 282

PRIMARY-EXAMINER: Grimley; Arthur T.

ASSISTANT-EXAMINER: Charioui; Mohamed

ATTY-AGENT-FIRM: Bracewell & Patterson L.L.P.

ABSTRACT:

A data processing system and method of monitoring the performance of a data processing system in processing data requests, where said data processing system processes data requests within a multilevel memory hierarchy. At least one token is passed with a data request along a particular path within the multilevel memory hierarchy. The time duration for the token to completely pass along the particular path is stored if expected conditions are encountered along the particular path within the multilevel memory hierarchy, such that the performance of said data processing system requesting data along that particular path under the expected conditions is determined and is available for subsequent performance monitoring.

46 Claims, 15 Drawing figures

L3: Entry 11 of 21 File: USPT Dec 21, 1999

DOCUMENT-IDENTIFIER: US 6006302 A
** See image for Certificate of Correction **
TITLE: Multiple bus system using a data transfer unit

Detailed Description Text (24):
FIG. 5 is a diagram showing the internal configuration of an embodiment of the data path switch 402 shown in FIG. 4. FIG. 5 includes data input/output drivers 507, 508, and 509 respectively connected to a processor data bus 413, a memory data bus; 416, and a system data bus 419; data latch circuits 501, 502, and 503; and data selectors 504, 505, and 506. A decoder 510 is disposed in this configuration to decode a data path control signal 420 produced from the bus-memory connection controller 401 so as to generate output enable signals 511, 512, and 513 respectively for the data I/O drivers 507, 508, and 509 as well as select signals 514, 515, and 516 respectively for the data selectors 504, 505, and 506.

Detailed Description Text (34):
FIG. 9 shows an example of relationships between the data path control signal 420 outputted from the bus-memory connection controller 401 to the data path switch 402, enable signals 511, 512, and 513 decoded by the decoder circuit 510 respectively for the I/O drivers 507, 508, and 509 in association with the control signal 420, and select signals 514, 515, and 516 for the data selectors 504, 505, and 506. In this diagram, the master, slave, and read/write fields in the upper-most row indicate a master unit, a slave unit, and a read or write request for a data transfer from the master unit to the slave unit, respectively. The remaining fields of the upper-most row includes signal names corresponding to the signals 511 to 516 of FIG. 5. Specifically, DT.sub.-- CNT in the right-most field of the row designates the data path control signal 420. This signal DT.sub.-- CNT includes three bits in this embodiment. In an idle state where data is not transferred, DT.sub.-- CNT 40 is set to 0 ("000").

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L3: Entry 11 of 21 File: USPT Dec 21, 1999

US-PAT-NO: 6006302
DOCUMENT-IDENTIFIER: US 6006302 A
**** See image for Certificate of Correction ****

TITLE: Multiple bus system using a data transfer unit

DATE-ISSUED: December 21, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Okazawa; Koichi	Tokyo			JP
Kimura; Koichi	Yokohama			JP
Kawaguchi; Hitoshi	Yokohama			JP
Aburano; Ichiharu	Hitachi			JP
Kobayashi; Kazushi	Ebina			JP
Mochida; Tetsuya	Yokohama			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 09/ 276968 [PALM]
DATE FILED: March 26, 1999

PARENT-CASE:
This is a continuation application of U.S. Ser. No. 09/143,985, filed Aug. 31, 1998; which is a continuation application of U.S. Ser. No. 08/959,913, filed Oct. 29, 1997 U.S. Pat. No. 5,889,971; which is a continuation application of U.S. Ser. No. 08/601,993, filed Feb. 15, 1996, now U.S. Pat. No. 5,751,976; which is a continuation application of U.S. Ser. No. 08/449,088, filed May 24, 1995, now U.S. Pat. No. 5,668,956; which is a continuation application of U.S. Ser. No. 08/311,893, filed Sep. 26, 1994, now U.S. Pat. No. 5,483,642; which is a continuation application of U.S. Ser. No. 07/705,701, filed May 23, 1991, now abandoned.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2-144301	June 4, 1990
JP	3-105536	October 5, 1991

INT-CL: [06] G06 F 13/14

US-CL-ISSUED: 710/129; 710/126
US-CL-CURRENT: 710/306

FIELD-OF-SEARCH: 710/126, 710/128, 710/129, 710/131

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PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4016546	April 1977	Bennett et al.	
☐	4439829	March 1984	Tsiang	
☐	4665483	May 1987	Ciacci et al.	
☐	4695944	September 1987	Zandveld et al.	
☐	4700348	October 1987	Ise et al.	
☐	4780813	October 1988	Gierety	
☐	4851990	July 1989	Johnson et al.	
☐	4945267	July 1990	Galbraith	
☐	4945540	July 1990	Kaneko	
☐	4982321	January 1991	Pantry et al.	
☐	5003465	March 1991	Chisholm et al.	
☐	5274795	December 1993	Vachon	
☐	5359715	October 1994	Heil et al.	
☐	5506973	April 1996	Okazawa et al.	

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
141302-A2	May 1985	EP	
191939-A1	August 1986	EP	
02-128250	May 1990	JP	

OTHER PUBLICATIONS

Glass, "Inside EISA", BYTE, vol. 14, No. 12, Nov. 1989, pp. 417-425.
Baran, "EISA Arrives", BYTE, vol. 14, No. 12, Nov. 1989, pp. 93-98.
"The Surging RISC", NIKKEI Electronics, No. 474, May 29,1989, pp. 106-119.

ART-UNIT: 271

PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Fay, Sharpe, Beall, Fagan, Minnich & McKee

ABSTRACT:

A processor bus linked with at least a processor, a memory bus linked with a main memory, and a system bus linked with at least an input/output device are connected

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to a three-way connection control system. The control system includes a bus-memory connection controller connected to address buses and control buses respectively of the processor, memory, and system buses to transfer address and control signals therebetween. The control system further includes a data path switch connected to data buses respectively of the processor, memory, and system buses to transfer data via the data buses therebetween depending on the data path control signal.

47 Claims, 19 Drawing figures

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L5: Entry 1 of 1 File: USPT Jun 5, 2001

DOCUMENT-IDENTIFIER: US 6243829 B1
TITLE: Memory controller supporting redundant synchronous memories

Detailed Description Text (37):
A first address-signal bus switch 290A is coupled to the address signal path 266A of the first memory bus 230A and to a second address-signal bus switch 290B associated with the second memory bus 230B. The first address-signal bus switch 290A is under the control of the first bus-switch control signal 288A that is generated by the first memory controller 224A. Likewise, the second address bus switch 290B is under the control of the second bus-switch control signal 288B which is generated from the second memory controller 224B. When both address-signal bus switches 290A, 290B are engaged, the data values of the first address signal 266A are transmitted to the address signal path 266B of the second memory bus 230B.

Detailed Description Text (38):
A first control-signal bus switch 292A is coupled to the control signal paths 264A, 268A of the first memory bus 230A and to a second control-signal bus switch 292B associated with the second memory bus 230B. The first control-signal bus switch 292A is under the control of the first bus-switch control signal 288A that is generated by the first memory controller 224A. Likewise, the second control-signal bus switch 290B is under the control of the second bus-switch control signal 288B which is generated from the second memory controller 224B. When both control-signal bus switches 290A, 290B are engaged, the values of the remote memory select control signal 264A are transmitted to the local memory select signal path 262B in the second memory bus 230B and the values of the read/write control signal 268A are transmitted to the read/write control signal path 268B in the second memory bus 230B.

Detailed Description Text (39):
A first data-signal bus switch 294A is coupled to the data signal path 225A of the first memory bus 230A and to a second data-signal bus switch 294B associated with the second memory bus 230B. The first data-signal bus switch 294A is under the control of the first bus-switch control signal 288A that is generated by the first memory controller 224A. Likewise, the second data-signal bus switch 294B is under the control of the second data-switch control signal 288B which is generated from the second memory controller 224B. When both data-signal bus switches 294A, 294B are engaged, the values of the first data signal 225A are transmitted to the data signal path 225B of the second memory bus 230B.

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End of Result Set

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L5: Entry 1 of 1 File: USPT Jun 5, 2001

US-PAT-NO: 6243829
DOCUMENT-IDENTIFIER: US 6243829 B1

TITLE: Memory controller supporting redundant synchronous memories

DATE-ISSUED: June 5, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Chan; Jong	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Company	Palo Alto	CA			02

APPL-NO: 09/ 085204 [PALM]
DATE FILED: May 27, 1998

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/7; 714/6, 714/5
US-CL-CURRENT: 714/7; 714/5, 714/6

FIELD-OF-SEARCH: 714/5-7, 714/707, 714/10, 714/11, 710/110, 711/162, 711/172

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5274645	December 1993	Idleman et al.	714/6
☐	5526507	June 1996	Hill	395/441
☐	5548711	August 1996	Brant	395/18203
☐	5625796	April 1997	Kaczmarczyk et al.	711/168
☐	5632013	May 1997	Krygowski et al.	714/7
☐	5790775	August 1998	Marks et al.	714/9
☐	5933653	August 1999	Ofek	714/5
☐	6021454	February 2000	Gibson	710/129

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☐	6041381	March 2000	Hoese	710/129
☐	6061772	May 2000	Webber et al.	711/169
☐	6073209	June 2000	Bergsten	711/114
☐	6073218	June 2000	DeKoning et al.	714/6
☐	6085333	July 2000	DeKoning et al.	714/7

ART-UNIT: 212

PRIMARY-EXAMINER: Lee; Thomas

ASSISTANT-EXAMINER: Nguyen; Nguyen

ABSTRACT:

A reliable fault-tolerant I/O controller supporting redundant synchronous memories is described. The I/O controller includes multiple I/O control logic units where each I/O control logic unit is in communication with a host server and external peripheral devices. Each I/O control logic unit includes a processor, a memory, and a memory controller. A master I/O control logic unit services I/O transactions from the host server and the external peripheral devices. A slave I/O control logic unit operates in a quiescent state until the master I/O control logic unit experiences a memory failure. At such time, the slave I/O control logic unit resumes operation of the I/O controller. In order to facilitate the switchover from the master I/O control logic unit to the slave I/O control logic unit, the master memory controller performs concurrent memory write operations in both the master and slave memories. The concurrent memory write operations ensure that the memories in both I/O control logic units are in a consistent state in order for the switchover to occur without loss of data.

17 Claims, 10 Drawing figures

L8: Entry 5 of 22 File: USPT Mar 21, 2000

DOCUMENT-IDENTIFIER: US 6040637 A
TITLE: Selector switch circuit for disabling an airbag

Abstract Text (1):
An airbag control system is provided to disable an airbag in a motor vehicle. The airbag control system includes an airbag control module, a switching circuit with a first circuit path and a second circuit path, and a switch selectively movable between an enabled position, which interconnects the first circuit path to the airbag control module to activate the airbag, and a disabled position, which interconnects the second circuit path to the airbag control module to prevent activation of the airbag. In addition, the system includes a third circuit path with a first resistor in series with a second resistor which is placed in parallel with a second contact of said switch. Alternatively, a controller is electrically connected through the third circuit path to the switch. The controller detects the position of the switch based on the resistance value it senses in the third circuit path. A visual indicator is optionally connected to the controller, whereby selectively moving the switch to the disabled position sends a signal from the controller to illuminate the visual indicator.

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L8: Entry 5 of 22 File: USPT Mar 21, 2000

US-PAT-NO: 6040637
DOCUMENT-IDENTIFIER: US 6040637 A

TITLE: Selector switch circuit for disabling an airbag

DATE-ISSUED: March 21, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Paganini; Lisa M.	Howell	MI		
Casilio; Frank	Troy	MI		
Peters; Roy	Almont	MI		
Straub; Kurt M.	Plymouth	MI		
DeHondt; Rene C.	Armada	MI		
Fry; Tova	Detroit	MI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Chrysler Corporation	Auburn Hills	MI			02

APPL-NO: 09/ 053037 [PALM]
DATE FILED: April 1, 1998

INT-CL: [07] B60 R 21/16

US-CL-ISSUED: 307/10.1; 280/728.1, 307/39
US-CL-CURRENT: 307/10.1; 280/728.1, 307/39

FIELD-OF-SEARCH: 307/9.1, 307/10.1, 307/39, 307/38, 307/85, 307/112, 307/113, 307/116, 307/121, 307/125, 307/139, 701/45, 701/36, 340/436, 340/438, 340/727, 280/728.1, 180/282, 180/283

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4346913	August 1982	Schrauf et al.	280/735
☐	4956631	September 1990	Itoh	340/436
☐	5165717	November 1992	Tanaka	

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☐	5318146	June 1994	Witte	
☐	5324074	June 1994	Christian et al.	
☐	5428340	June 1995	Kawabuta et al.	
☐	5460404	October 1995	Damisch et al.	280/735
☐	5541523	July 1996	Tourville et al.	324/711
☐	5544914	August 1996	Borninski et al.	
☐	5564737	October 1996	Ito et al.	280/735

ART-UNIT: 286

PRIMARY-EXAMINER: Gaffin; Jeffrey

ASSISTANT-EXAMINER: Huynh; Kim

ATTY-AGENT-FIRM: Fuller, III; Roland A.

ABSTRACT:

An airbag control system is provided to disable an airbag in a motor vehicle. The airbag control system includes an airbag control module, a switching circuit with a first circuit path and a second circuit path, and a switch selectively movable between an enabled position, which interconnects the first circuit path to the airbag control module to activate the airbag, and a disabled position, which interconnects the second circuit path to the airbag control module to prevent activation of the airbag. In addition, the system includes a third circuit path with a first resistor in series with a second resistor which is placed in parallel with a second contact of said switch. Alternatively, a controller is electrically connected through the third circuit path to the switch. The controller detects the position of the switch based on the resistance value it senses in the third circuit path. A visual indicator is optionally connected to the controller, whereby selectively moving the switch to the disabled position sends a signal from the controller to illuminate the visual indicator.

12 Claims, 3 Drawing figures

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L8: Entry 14 of 22 File: USPT Dec 10, 1991

DOCUMENT-IDENTIFIER: US 5072441 A
TITLE: Packet switched information network with universal access to enhanced network services

Abstract Text (1):
An information network for connecting input communication devices using a number of different access protocols to network hosts in which a packet switch is provided for enabling and disabling communication paths betweeen the input devices and hosts and in which an enhanced network function server is able to be used during operation of the packet switch by an enhanced network function access module which permits access to the enhanced function server for the different access protocols.

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L8: Entry 14 of 22 File: USPT Dec 10, 1991

US-PAT-NO: 5072441
DOCUMENT-IDENTIFIER: US 5072441 A

TITLE: Packet switched information network with universal access to enhanced network services

DATE-ISSUED: December 10, 1991

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Szwarc; Michal	Valley Cottage	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Nynex Corporation	New York	NY			02

APPL-NO: 07/ 563704 [PALM]
DATE FILED: August 7, 1990

INT-CL: [05] H04Q 11/04

US-CL-ISSUED: 370/60; 370/94.1, 370/15
US-CL-CURRENT: 370/389; 370/466

FIELD-OF-SEARCH: 370/60, 370/94.1, 370/15

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	293850	December 1987	Kolsumata	370/60
☐	2189112	October 1987	Carter et al.	370/60
☐	4760395	July 1988	Katreff et al.	370/60
☐	4951278	August 1990	Biber et al.	370/94.1

ART-UNIT: 263

PRIMARY-EXAMINER: Olms; Douglas W.

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ASSISTANT-EXAMINER: Samuel; T.

ATTY-AGENT-FIRM: Kirk; Douglas J. Torrente; John J.

ABSTRACT:

An information network for connecting input communication devices using a number of different access protocols to network hosts in which a packet switch is provided for enabling and disabling communication paths betweeen the input devices and hosts and in which an enhanced network function server is able to be used during operation of the packet switch by an enhanced network function access module which permits access to the enhanced function server for the different access protocols.

24 Claims, 10 Drawing figures

L15: Entry 5 of 11 File: USPT Mar 7, 2000

DOCUMENT-IDENTIFIER: US 6034956 A
TITLE: Method of simultaneously attempting parallel path connections in a multi-stage interconnection network

Detailed Description Text (6):
The path selection command comprises a specification of the eight output ports 14(1)-14(8) (and hence the eight alternate paths) that the switch 10 should choose from in routing the data subsequently received over lines DATA1-DATA8 at the input port 12 where the command was received. The path selection command is transmitted to the switch 10 during a switch set-up time period and, in accordance with the path selection method, there is a one-to-one corresponding relationship between the enabling or disabling of a data line (DATA1-DATA8) and the enabling or disabling of an output port 14(1)-14(8) for consideration and possible connection. By this it is meant that the transmission over DATA1 enables (with a logic high) or disables (with a logic low) output port 14(1) with respect to a connection to the input port; DATA2 enables or disables output port 12(2) with respect to a connection to the input port; DATA3 enables or disables output port 12(3) with respect to a connection to the input port; and so on. Accordingly, each active (logic high) data line enables the corresponding output port 14 as an allowable path selection for data transmission, while each inactive data line disables the corresponding output port 14 as an allowable path selection.

Current US Cross Reference Classification (8):
710/316

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L15: Entry 5 of 11 File: USPT Mar 7, 2000

US-PAT-NO: 6034956
DOCUMENT-IDENTIFIER: US 6034956 A

TITLE: Method of simultaneously attempting parallel path connections in a multi-stage interconnection network

DATE-ISSUED: March 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Olnowich; Howard Thomas	Endwell	NY		
Bruck; Jehoshua	La Canada	CA		
Fisher; Michael Hans	Rochester	MN		
Gould; Joel Mark	Winchester	MA		
Jabusch; John David	Cary	NC		
Williams; Arthur Robert	Croton-On-Hudson	NY		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
International Business Machines Corporation	Armonk	NY			02

APPL-NO: 09/ 106960 [PALM]
DATE FILED: June 29, 1998

PARENT-CASE:
CROSS-REFERENCE TO RELATED APPLICATIONS This application for patent is related to the following prior applications for patent: U.S. Ser. No. 07/947,023, filed Sep. 17, 1992 entitled "Adaptive Switching Apparatus for Multi-Stage Networks" by Howard T. Olnowich, et al. now U.S. Pat. No. 5,345,229; U.S. Ser. No. 07/677,543, filed Mar. 29, 1991, entitled "All-Node Switch, An Unclocked, Unbuffered Asynchronous Switching Apparatus" by P. A. Franaszek, et al. now abandoned; U.S. Ser. No. 07/799,497, filed Nov. 27, 1991, entitled "Multi-Function Network" by Howard T. Olnowich, et al. now U.S. Pat. No. 5,654,695; and This application for patent is also related to the following application for patent filed concurrently herewith: U.S. Ser. No. 08/481,855, filed, Jun. 7, 1995, entitled "Multi-Stage Interconnection Network with Selectable Function Switching Apparatus" by Howard T. Olnowich, et al. (IBM # EN9-94-021) now U.S. Pat. No. 5,835,024. This application is a divisional of Ser. No. 08/950,104 filed on Oct. 16, 1997, entitled "Flash-Flooding Multi-Stage Interconnection Network with Parallel Path Seeking Switching Elements" (Olnowich et at) now U.S. Pat. No. 5,774,067, which is a continuation under 37 CFR 1.62 of parent application, Ser. No. 08/481,854, filed on Jun. 7, 1995, also entitled "Flash-Flooding Multi-Stage Interconnection Network with Parallel Path Seeking Switching Elements" (Olnowich et al) now U.S. Pat. No. 5,835,024. The disclosures of each of the foregoing applications for patent are hereby incorporated by reference herein for all permissible purposes.

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INT-CL: [07] H04 Q 1/00, H04 L 12/28, G06 F 13/00, H04 M 3/00, H04 M 7/00

US-CL-ISSUED: 370/388; 340/825.8, 340/827, 370/397, 370/399, 370/359, 395/311, 379/221, 379/272, 379/292, 710/131
US-CL-CURRENT: 370/388; 340/2.6, 370/359, 370/397, 370/399, 379/221.01, 379/272, 379/292, 710/316

FIELD-OF-SEARCH: 340/825.79, 340/825.03, 340/825.8, 340/826, 340/825.89, 340/827, 370/388, 370/398, 370/397, 370/399, 370/381, 370/379, 370/359, 326/41, 326/38, 395/312, 395/311, 395/182.02, 379/219, 379/220, 379/221, 379/224, 379/268, 379/271, 379/272, 379/273, 379/291, 379/292, 379/306, 710/131, 710/132, 714/4

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4630260	December 1986	Toy et al.	370/388 X
☐	4656622	April 1987	Lea	370/388 X
☐	4661947	April 1987	Lea et al.	370/388 X
☐	4679190	July 1987	Dias et al.	370/388 X
☐	4696000	September 1987	Payne et al.	370/388 X
☐	4821034	April 1989	Anderson et al.	340/825.8
☐	4953162	August 1990	Lyons et al.	370/94.1
☐	4965788	October 1990	Newman	370/60
☐	5040173	August 1991	Richards	370/54
☐	5056085	October 1991	Vu	370/60
☐	5117422	May 1992	Hauptschein et al.	370/95.1
☐	5119366	June 1992	Ardon et al.	370/54
☐	5144297	September 1992	Ohara	340/825.89 X
☐	5155433	October 1992	Baran et al.	370/94.3
☐	5181017	January 1993	Frey, Jr. et al.	340/825.02
☐	5237565	August 1993	Henrion et al.	340/826 X
☐	5345229	September 1994	Olnowich et al.	340/825.8
☐	5367518	November 1994	Newman	340/826 X
☐	5444705	August 1995	Olnowich et al.	370/388
☐	5469154	November 1995	Karp	340/825.8
☐	5542048	July 1996	Olnowich et al.	340/825.8 X
☐	5555243	September 1996	Kakuma et al.	340/826 X
☐	5774067	June 1998	Olnowich et al.	340/827

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OTHER PUBLICATIONS

IPM.RTM. Technical Disclosure Bulletin: Asynchronous Digital Video Switching System, Oct. 1990, vol. 33 No. 5, pp. 227-233.
IPM .RTM. Technical Disclosure Bulletin: XNL Switch and its Control, Jan. 1992, vol. 34 No. 8, pp. 16-21.

APT-UNIT: 275

PRIMARY-EXAMINER: Horabik; Michael

ASSISTANT-EXAMINER: Wilson, Jr.; William H.

ATTY-AGENT-FIRM: Beckstrand; Shelley M

ABSTRACT:

The multi-stage interconnection network of the present invention includes the use of switches in the first stage that have parallel path seeking capabilities. With these switches, a directed flash-flood can be instigated from any one node wherein multiple paths through the network to a designated destination node are tried in parallel in an attempt to find a connection path therebetween. The switches in the first and second stages are interconnected such that each switch in the first stage is connected with every possible priority level to the switches of the second stage. The parallel path seeking switches and network are further configured to test for rejection of the flash-flood by monitoring all connections in combination.

19 Claims, 18 Drawing figures

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US-PAT-NO: 6581136

DOCUMENT-IDENTIFIER: US 6581136 B1

TITLE: Fibre channel data storage system having expansion/contraction

---------- KWIC ---------

Brief Summary Text - BSTX (2):

This invention relates generally to data storage systems and more particularly to data storage systems having a plurality of magnetic storage disk drives in a redundancy arrangement whereby the disk drives are controllable by first disk controllers and second disk controllers. Still more particularly, the invention also relates to systems of such type wherein the disk drives are coupled to the disk controllers through a series, unidirectional, "ring" or, fibre channel protocol, communication system.

Brief Summary Text - BSTX (3):

As is known in the art, in one type of data storage system, data is stored in a bank of magnetic storage disk drives. The disk drives, and their coupled interfaces, are arranged in sets, each set being controlled by a first disk controller and a second disk controller. More particularly, in order to enable the set of disk drives to operate in the event that there is a failure of the first disk controller, each set is also coupled to a second, or redundant disk controller. Therefore, if either the first or second disk controller fails, the set can be accessed by the other one of the disk controllers.

Current US Cross Reference Classification - CCXR (3):

710/316

US006581136B1

(12) **United States Patent**
Tuccio et al.

(10) **Patent No.: US 6,581,136 B1**
(45) **Date of Patent: Jun. 17, 2003**

(54) **FIBRE CHANNEL DATA STORAGE SYSTEM HAVING EXPANSION/CONTRACTION**

(75) Inventors: **William R. Tuccio, Sutton, MA (US); Thomas Earl Linnell, Northborough, MA (US); Christopher J. Mulvey, Shrewsbury, MA (US)**

(73) Assignee: **EMC Corporation, Hopkinton, MA (US)**

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/345,048**

(22) Filed: **Jun. 30, 1999**

(51) Int. Cl.[7] **G06F 12/00**

(52) U.S. Cl. **711/114; 370/362; 370/360; 710/316**

(58) Field of Search 710/11, 5, 131, 710/129, 28, 38, 316; 711/114, 112, 100; 714/6, 8, 7, 42, 43, 44; 370/357, 359, 360, 351, 362

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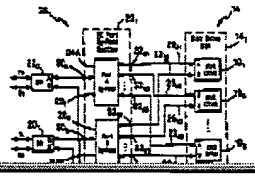
(List continued on next page.)

Primary Examiner—Matthew Kim
Assistant Examiner—Pierre Michel Bataille
(74) *Attorney, Agent, or Firm*—Daly, Crowley & Mofford, LLP

(57) **ABSTRACT**

A data storage system having a plurality of disk drives. Each one has a pair of ports. A pair of directors controls the flow of data to and from the disk drives. A first fibre channel port by-pass selector section is provided. The first fibre channel selector section includes: an input/output port coupled to a first one of the directors; and, a plurality of output/input ports connected between a first one of the ports of the plurality of disk drives through a first plurality of fibre channel links. The first fibre channel port by-pass selector section is adapted to couple the first one of the directors serially to one, or ones, of the first ports of the plurality of disk drives through a first fibre channel selectively in accordance with a control signal fed to the first fibre channel by-pass selector section. The first fibre channel includes one, or more, of the first plurality of fibre channel links. A second fibre channel port by-pass selector section is provided having an input/output port coupled to a second one of the directors and a plurality of output/ports serially connected between a second one of the pair of ports of the plurality of disk drives through a second plurality of fibre channel links. The second fibre channel port by-pass selector section is adapted to couple the second one of the directors serially to one, or ones, of the second ports of the plurality of disk drives through a second fibre channel selectively in accordance with the control signal. The second fibre channel includes one, or more, of the second plurality of fibre channel links.

4 Claims, 22 Drawing Sheets



US-PAT-NO: 6338110

DOCUMENT-IDENTIFIER: US 6338110 B1

TITLE: Partitioning of storage channels using programmable switches

---------- KWIC ---------

Brief Summary Text - BSTX (17):

According to another embodiment of the invention, a data storage system, comprises a first storage channel, a first controller coupled to the first storage channel, a first storage device coupled to the first storage channel, a second storage channel, a second controller coupled to the second storage channel, a second storage device coupled to the second storage channel, a third storage channel coupled to the first controller and the first storage device, a fourth storage channel coupled to the second controller and the second storage device, and a switch coupled to the first storage channel and the second storage channel. The switch separates the first storage channel from the second storage channel in a first state and connects the first storage channel and the second storage channel in a second state.

Claims Text - CLTX (10):

wherein the second controller is configured to control the first storage device and the second storage device in response to detection of failure of the first controller.

Claims Text - CLTX (28):

17. The data storage system of claim 1, comprising logic that causes entry of the switch into the first state if a signal is received from the first controller and the second controller.

Claims Text - CLTX (29):

18. The data storage system of claim 1, comprising logic that causes entry of the switch into the second state and activation of mirroring of data between the first controller and the second controller.

US006338110B1

(12) **United States Patent**
van Cruyningen

(10) **Patent No.: US 6,338,110 B1**
(45) **Date of Patent: *Jan. 8, 2002**

(54) **PARTITIONING OF STORAGE CHANNELS USING PROGRAMMABLE SWITCHES**

(75) Inventor: Peter van Cruyningen, San Jose, CA (US)

(73) Assignee: Sun Microsystems, Inc., Palo Alto, CA (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 09/162,109

(22) Filed: Sep. 28, 1998

Related U.S. Application Data

(60) Provisional application No. 60/065,914, filed on Nov. 14, 1997.

(51) Int. Cl.[7] G06F 13/00

(52) U.S. Cl. 710/131; 710/129; 710/109

(58) Field of Search 710/131, 129, 710/126, 109

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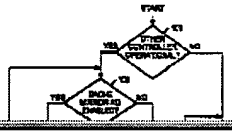
Primary Examiner—Ario Etienne
(74) *Attorney, Agent, or Firm*—Conley, Rose & Tayon, PC; B. Noël Kivlin

(57) **ABSTRACT**

A data storage system having a first storage channel, a first controller coupled to the first storage channel, a first storage device coupled to the first storage channel, a second storage channel, a second storage device coupled to the second storage channel, and a switch coupled to the first storage channel and the second storage channel. The switch separates the first storage channel from the second storage channel in a first state and connects the first storage channel and the second storage channel in a second state. Also described is a method of controlling a data storage system having a first storage channel, a first storage device coupled to the first storage channel, an operational controller coupled to the first storage channel, a second storage channel, a second storage device coupled to the second storage channel, and a switch coupled to the first storage channel and the second storage channel. The method includes detecting whether an operational controller is coupled to the second storage channel and if an operational controller is coupled to the second storage channel, then opening the switch.

47 Claims, 6 Drawing Sheets



US-PAT-NO: 6272533

DOCUMENT-IDENTIFIER: US 6272533 B1

TITLE: Secure computer system and method of providing secure access to a computer system including a stand alone switch operable to inhibit data corruption on a storage device

---------- KWIC ---------

Brief Summary Text - BSTX (23):

According to another feature of the invention, the digital computer system further includes first and second disk controllers connected to respective master and slave central processing units by a system bus. The secure data storage device includes a first disk drive electrically connected through the manually operative switch to the first disk controller for receiving a control signal from the master central processing unit whereby the manually operative switch selectively enables and disables transmission of the control signal to the first disk drive. The second disk drive is connected to the second disk controller and is accessible by the master and slave central processing units over the system bus. Alternatively, the first and second disk controllers may be included on separate buses accessible only by the respective master and slave central processing units.

Brief Summary Text - BSTX (29):

According to another feature of the invention, the processor includes a first disk controller and the data storage device is a first disk drive. According to another feature of the invention, a second disk drive may also be connected to the first disk controller or may be connected to its own, second disk controller.

Claims Text - CLTX (24):

first and second controllers respectively connected to said master and slave central processing units by respective ones of said system buses;

US006272533B1

(12) **United States Patent**
Browne

(10) **Patent No.: US 6,272,533 B1**
(45) **Date of Patent: Aug. 7, 2001**

(54) **SECURE COMPUTER SYSTEM AND METHOD OF PROVIDING SECURE ACCESS TO A COMPUTER SYSTEM INCLUDING A STAND ALONE SWITCH OPERABLE TO INHIBIT DATA CORRUPTION ON A STORAGE DEVICE**

(76) Inventor: **Hendrik A. Browne**, 6211 Florence Way, Alexandria, VA (US) 22310

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/250,277**

(22) Filed: **Feb. 16, 1999**

(51) Int. Cl.[7] **G06F 13/38**

(52) U.S. Cl. 709/213; 710/128; 711/152; 711/100; 711/111; 711/154

(58) Field of Search 711/100, 111, 711/112, 154, 152; 360/60; 710/128, 131; 709/213

(56) **References Cited**

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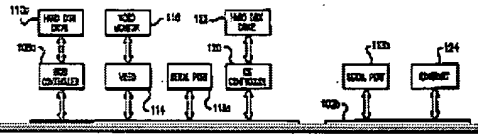
(74) *Attorney, Agent, or Firm*—Fulbright & Jaworski LLP

(57) **ABSTRACT**

A computer system includes hardware for selectively disabling alteration of data residing on a mass storage device which is subject to remote access. In one embodiment, a hard disk drive is operated in a conventional manner including both read and write modes when the system is being operated in a non-secure mode of operation, such as when remote access is not allowed. In a secure mode of operation, a locally operated switch is used to disable writing to the hard disk drive to maintain data integrity on the drive. The system may also include first and second electrically isolated buses and corresponding processors. In this configuration, the hard disk drive may be selectively connected to the first bus and processor for the storage of data, or to the second bus and processor when in a secure mode to provide for read-only remote access to the information stored on the hard drive. A write-only hard drive may also be included for storage of confidential information provided by remote users so that other remote users cannot access that information. In a master/slave processor configuration, all system programming is resident in an isolated portion of the system inaccessible to remote users. The slave processor receives instructions only from the master processor so that the operation of the slave processor cannot be compromised by viruses uploaded by remote users.

45 Claims, 9 Drawing Sheets



Detailed Description Text - DETX (85):

FIG. 17A is a schematic diagram of an essentially point-to-point architecture scheme showing the invalidate request and invalidate acknowledge signals. The exemplary embodiment is shown generally at 1500. A first storage controller 1502 is coupled to instruction processor 1506 and instruction processor 1508 via interfaces 1510 and 1512, respectively. A second storage controller 1504 is coupled to an instruction processor 1518 and an instruction processor 1520 via interfaces 1522 and 1524, respectively. Storage controller 1502 and storage controller 1504 may be coupled together in an essentially point-to-point architecture generally as shown in FIG. 1 and discussed with reference thereto.

Detailed Description Text - DETX (90):

FIG. 18A is a schematic diagram of a system utilizing the XBAR interface block showing the invalidate request and invalidate acknowledge signals. The schematic diagram is generally shown at 1550. A first storage controller 1554 is coupled to an instruction processor 1556 and an instruction processor 1558 via interfaces 1560 and 1562, respectively. A second storage controller 1670 is coupled to an instruction processor 1576 and an instruction processor 1578 via interfaces 1580 and 1582, respectively. Storage controller 1554 may be coupled to XBAR interface block 1564 in accordance with FIGS. 2-16 and the discussion relating thereto. Similarly, storage controller 1670 may be coupled to XBAR interface block 1564 in accordance with FIGS. 2-16 and the discussion relating thereto.

Detailed Description Text - DETX (94):

FIG. 19A is a schematic diagram of a system utilizing the XBAR interface block showing the anticipatory acknowledge signal of the present invention. The schematic diagram is generally shown at 1620. A first storage controller 1624 is coupled to an instruction processor 1626 and an instruction processor 1628 via interfaces 1630 and 1632, respectively. A second storage controller 1648 is coupled to an instruction processor 1650 and an instruction processor 1652 via interfaces 1654 and 1656, respectively. Storage controller 1624 may be coupled to XBAR interface block 1634 in accordance with FIGS. 2-16 and the discussion relating thereto. Similarly, storage controller 1648 may be coupled to XBAR interface block 1634 in accordance with FIGS. 2-16 and the discussion relating thereto.

Current US Cross Reference Classification - CCXR (1):

710/317

US-PAT-NO: 5289589

DOCUMENT-IDENTIFIER: US 5289589 A
See image for Certificate of Correction

TITLE: Automated storage library having redundant SCSI bus system

--------- KWIC ---------

Claims Text - CLTX (7):
a switch having a first and second side, a first transceiver on the first side of the switch and coupled to the first controller, a second transceiver on the first side of the switch and coupled to the second controller, a third transceiver on the second side of the switch and coupled to the peripheral storage device, anti-latch circuits coupled between the first, second, and third transceivers, and switch control logic coupled to the transceivers for selectively coupling a transceiver on the first side of the switch to the third transceiver, the picker and peripheral storage device coupled to the second side of the switch by at least one SCSI bus;

Claims Text - CLTX (56):
means coupled to the first controller for preventing the first controller from addressing some of the third and fourth pluralities of peripheral storage devices and for preventing the second controller from addressing some of the first and second pluralities of peripheral storage devices.

Current US Original Classification - CCOR (1):
710/316

US005289589A

United States Patent [19]

Bingham et al.

[11] Patent Number: 5,289,589

[45] Date of Patent: Feb. 22, 1994

[54] **AUTOMATED STORAGE LIBRARY HAVING REDUNDANT SCSI BUS SYSTEM**

[75] Inventors: Robert L. Bingham; Kamal R. Dimitri, both of Tucson, Ariz.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 579,805

[22] Filed: Sep. 10, 1990

[51] Int. Cl.[5] G06F 13/40

[52] U.S. Cl. 395/425; 395/575; 395/325; 364/240; 364/240.5; 364/248.1; 364/DIG. 1

[58] Field of Search 395/275, 800, 325, 425, 395/575; 369/291; 358/86; 364/423

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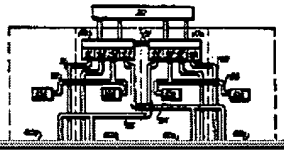
Primary Examiner—Thomas C. Lee
Assistant Examiner—Paul R. Lintz
Attorney, Agent, or Firm—M. W. Schecter

[57] **ABSTRACT**

An optical disk library having a redundant SCSI bus system which utilizes double-sided, multi-ported switches for connecting each of two library controllers to all library pickers and some or all of the optical disk drives in the library is disclosed. The use of additional library controllers and pickers allows for greater subsystem flexibility and redundancy. The switches minimize the need for additional SCSI adapters to the library controllers and include anti-latch circuitry between sets of transceivers to eliminate the need to know the direction of data flow on a bus. In addition, the switches are physically located apart from the SCSI adapters, pickers, and optical disk drives, thereby minimizing the amount of customization required, and permit switching from the primary library controller to the secondary library controller to provide access to any optical disk in the library when a failure in the system has otherwise made such optical disk inaccessible through the primary library controller. The pickers and optical disk drives are coupled to the switches in one or more singleended strings to simplify library operations and minimize the amount of the library made inoperative by a device failure. Each picker is coupled to the switches on a single-ended string to which no optical disk drive is attached, further reducing the likelihood that access to optical disks in the library will be lost during a failure.

18 Claims, 4 Drawing Sheets



First Hit Fwd Refs

Generate Collection Print

L4: Entry 2 of 33 File: USPT Dec 9, 2003

DOCUMENT-IDENTIFIER: US 6662282 B2
TITLE: Unified data sets distributed over multiple I/O-device arrays

Brief Summary Text (5):
FIG. 1 is a block diagram of a standard disk drive. The disk drive 101 receives I/O requests from remote computers via a communications medium 102 such as a computer bus, fibre channel, or other such electronic communications medium. For many types of storage devices, including the disk drive 101 illustrated in FIG. 1, the vast majority of I/O requests are either read or WRITE requests. A READ request requests that the storage device return to the requesting remote computer some requested amount of electronic data stored within the storage device. A WRITE request requests that the storage device store electronic data furnished by the remote computer within the storage device. Thus, as a result of a read operation carried out by the storage device, data is returned via communications medium 102 to a remote computer, and as a result of a write operation, data is received from a remote computer by the storage device via communications medium 102 and stored within the storage device.

Brief Summary Text (9):
Electronic data is stored within a disk array at specific addressable locations. Because a disk array may contain many different individual disk drives, the address space represented by a disk array is immense, generally many thousands of gigabytes. The overall address space is normally partitioned among a number of abstract data storage resources called logical units ("LUNs"). A LUN includes a defined amount of electronic data storage space, mapped to the data storage space of one or more disk drives within the disk array, and may be associated with various logical parameters including access privileges, backup frequencies, and mirror coordination with one or more LUNs. LUNs may also be based on random access memory ("RAM"), mass storage devices other than hard disks, or combinations of memory, hard disks, and/or other types of mass storage devices. Remote computers generally access data within a disk array through one of the many abstract LUNs 208-215 provided by the disk array via internal disk drives 203-205 and the disk array controller 206. Thus, a remote computer may specify a particular unit quantity of data, such as a byte, word, or block, using a bus communications media address corresponding to a disk array, a LUN specifier, normally a 64-bit integer, and a 32-bit, 64-bit, or 128-bit data address that specifies a LUN, and a data address within the logical data address partition allocated to the LUN. The disk array controller translates such a data specification into an indication of a particular disk drive within the disk array and a logical data address within the disk drive. A disk drive controller within the disk drive finally translates the logical address to a physical medium address. Normally, electronic data is read and written as one or more blocks of contiguous 32-bit or 64-bit computer words, the exact details of the granularity of access depending on the hardware and firmware capabilities within the disk array and individual disk drives as well as the operating system of the remote computers generating I/O requests and characteristics of the communication medium interconnecting the disk array with the remote computers.

Brief Summary Text (10):
In many computer applications and systems that need to reliably store and retrieve

data from a mass storage device, such as a disk array, a primary data object, such as a file or database, is normally backed up to backup copies of the primary data object on physically discrete mass storage devices or media so that if, during operation of the application or system, the primary data object becomes corrupted, inaccessible, or is overwritten or deleted, the primary data object can be restored by copying a backup copy of the primary data object from the mass storage device. Many different techniques and methodologies for maintaining backup copies have been developed. In one well-known technique, a primary data object is mirrored. FIG. 3 illustrates object-level mirroring. In FIG. 3, a primary data object "O.sub.3 " 301 is stored on LUN A 302. The mirror object, or backup copy, "O.sub.3 " 303 is stored on LUN B 304. The arrows in FIG. 3, such as arrow 305, indicate I/O write operations directed to various objects stored on a LUN. I/O write operations directed to object "O.sub.3 " are represented by arrow 306. When object-level mirroring is enabled, the disk array controller providing LUNs A and B automatically generates a second I/O write operation from each I/O write operation 306 directed to LUN A, and directs the second generated I/O write operation via path 307, switch "S.sub.1 " 308, and path 309 to the mirror object "O.sub.3 " 303 stored on LUN B 304. In FIG. 3, enablement of mirroring is logically represented by switch "S.sub.1 " 308 being on. Thus, when object-level mirroring is enabled, any I/O write operation, or any other type of I/O operation that changes the representation of object "O.sub.3 " 301 on LUN A, is automatically mirrored by the disk array controller to identically change the mirror object "O.sub.3 " 303. Mirroring can be disabled, represented in FIG. 3 by switch "S.sub.1 " 308 being in an off position. In that case, changes to the primary data object "O.sub.3 " 301 are no longer automatically reflected in the mirror object "O.sub.3 " 303. Thus, at the point that mirroring is disabled, the stored representation, or state, of the primary data object "O.sub.3 " 301 may diverge from the stored representation, or state, of the mirror object "O.sub.3 " 303. Once the primary and mirror copies of an object have diverged, the two copies can be brought back to identical representations, or states, by a resync operation represented in FIG. 3 by switch "S.sub.2 " 310 being in an on position. In the normal mirroring operation, switch "S.sub.2 " 310 is in the off position. During the resync operation, any I/O operations that occurred after mirroring was disabled are logically issued by the disk array controller to the mirror copy of the object via path 311, switch "S.sub.2," and pass 309. During resync, switch "S.sub.1 " is in the off position. Once the resync operation is complete, logical switch "S.sub.2 " is disabled and logical switch "S.sub.1 " 308 can be turned on in order to reenable mirroring so that subsequent I/O write operations or other I/O operations that change the storage state of primary data object "O.sub.3," are automatically reflected to the mirror object "O.sub.3 " 303.

L4: Entry 4 of 33 File: USPT Jan 14, 2003

DOCUMENT-IDENTIFIER: US 6507581 B1
TITLE: Dynamic port mode selection for crosspoint switch

Brief Summary Text (5):
U.S. Pat. No. 5,710,550 entitled "Apparatus for Programmable Signal Switching" issued Jan. 20, 1998 to Hsieh et al ('550), describes a crossbar (or crosspoint) switch having a set of input/output (I/O) terminals interconnected by an array of pass transistors, one for each possible pair of I/O terminals. Each pass transistor links the corresponding pair of I/O terminals so that when the transistor is turned on, it provides a bidirectional signal path between those two I/O terminals. The crosspoint switch also includes a random access memory (RAM) storing a data word corresponding to each I/O terminal. Each bit of the data word controls the on/off state of a pass transistor linking that I/O terminal to some other I/O terminal. An external host computer can make or break routing paths by writing data to various RAM addresses. A serial bus links the host computer to a memory controller. When the host computer sends routing control data and a RAM address to the memory controller via the serial bus, the memory controller writes that data to the routing control RAM, thereby making and/or breaking routing paths to the switch port corresponding to that address.

Brief Summary Text (6):
When a crosspoint switch is used in some high speed applications, it is important that host computer be able to quickly command the crosspoint switch to make or break a routing path. To specify a routing path change, the host computer must send a relatively large amount of data over the serial bus. It therefore takes a relatively long time for a routing path change to occur once the host computer decides it wants to make the path change. To speed up routing data transfer, Hsieh's system includes a parallel bus linking the host computer to the memory controller. The parallel bus is made wide enough to convey all of the information the memory controller needs to write a word to the RAM controlling routing paths through the crosspoint switch. This system therefore enables the host computer to command a routing change in one parallel bus data cycle. However since the width of the parallel bus is proportional to the number of switch terminals, the required parallel bus width becomes impractically large as the number of switch terminals increases.

Brief Summary Text (7):
A crosspoint switch is useful for selectively routing both digital and analog signals between lines or buses connected to its terminals. However since a pass transistor can degrade a digital signal, it is helpful to provide a port at each I/O terminal that can buffer a signal before it enters the switch at that terminal or after it departs the switch from the terminal. U.S. Pat. No. 5,734,334 entitled "Programmable Port for Crossbar Switch" issued Mar. 31, 1998 to Hsieh et al ('334) describes a crossbar (crosspoint) switch having a port at each of its terminals. Each port may operate in either an analog mode or in any one of several digital modes depending on the type of signal being routed through the crosspoint switch. In its analog mode the port simply passes an analog signal entering or leaving the crosspoint switch terminal without buffering it. In all digital modes the port buffers any digital signal entering or leaving the switch terminal. In a digital bidirectional mode, the port buffers digital signals both entering and leaving the

port terminal. In a unidirectional input mode, the port buffers signals entering the terminal and blocks signals leaving the terminal. Conversely, in a unidirectional output mode, the port buffers signals leaving the terminal but block signals arriving at the terminal. The port also has tristate bidirectional and unidirectional mode in which signals are buffered only when an externally generated tristate control signal is asserted. A set of tristate control lines are provided in parallel to each port and each port may be programmed to select any one of those lines as its tristate control input. A host computer can change the operating mode of any port or select its source of tristate control signal by transmitting programming data to that port through a serial bus linking the host computer to all switch ports. That same serial bus also delivers routing data from the host computer to the memory controller for the routing control RAM.

Brief Summary Text (8):
In some high speed applications, it would be beneficial if the host computer could not only quickly make or break a routing path between two ports but also to quickly change the operating modes of the two ports. However, in the system described by the '334 patent, since the host computer must transmit the routing control data and the port mode control data over the same serial bus, the operation cannot be carried out quickly. Even when the number of switch terminals is small enough that it is practical to send routing control data via a parallel bus as taught by the '550 patent, the time the host requires to transmit mode control data to the two ports involved in a routing change extends the overall time needed to carry out that routing change.

Drawing Description Text (5):
FIG. 3 illustrates the parallel bus interface circuit of FIG. 2 in more detailed block diagram form;

Detailed Description Text (8):
SRAM 14 is a static random access memory having 160 addressable storage locations, each for storing a data word including a 0 to 159 bit routing data field Sx and a 2-bit port mode control field Cx. SRAM 14, accessed via a 162-bit parallel data bus (DATA) and a 160 word select bus (WORD), replaces one of its stored data words (Sx, Cx) with a word appearing on the DATA bus whenever one of the WORD lines is asserted. The particular WORD line being asserted indicates the SRAM address to which the word on the DATA bus is to be written.

Detailed Description Text (9):
To initially program switch 10, an external host controller sends a serial data sequence to control interface circuit 16 via an IEEE standard JTAG serial bus. The data sequence includes a data word (Sx, Cx) for each address of SRAM 14, programming data to be supplied to each port P0-P159 and other programming data as described below. Control interface circuit 16 sequentially places the incoming (Sx, Cx) words on the DATA bus input to SRAM 14 and strobes each WORD bus line in succession to write each incoming (Sx, Cx) data word to a separate SRAM 14 address. As described below, control interface circuit 16 also internally stores some of the serial data arriving on the JTAG bus for guiding its own behavior thereafter

Detailed Description Text (10):
After the host computer initially programs switch 10 by sending data transferred to control interface circuit 16 via the JTAG bus, it may at any time thereafter make or break a connection between a pair of ports P0-P159 and set their operating modes by sending a single command to control interface circuit 16 via a conventional parallel data bus (PARALLEL). The command is an 8-bit data word that is encoded to identify the two ports, to indicate whether a connection between the two ports is to be made or broken, and to indicate the values of the port operating mode fields Cx to be supplied to the two ports. Upon receiving the command, control interface circuit 16 writes appropriate (Sx, Cx) words to the two addresses of SRAM 14 that correspond to the two ports. For example if port P0 is to be connected to port

P158, control interface circuit 16 writes a word to address 0 of SRAM 14 establishing the connection between ports P0 and P158 through switch array 12 and also appropriately setting the operating mode of port P0. Control interface circuit 16 then writes a word to address 158 of SRAM 14 breaking any other connection to port P158 and appropriately setting the operating mode of port P158.

Detailed Description Text (11):
The host computer can therefore not only make or break a connection between any two ports P0-P159 in one write cycle of the PARALLEL bus, it can also set the operating mode of both ports. Since there are 12,720 possible pairs of ports P0-P159, the command conveyed on the PARALLEL bus could use 14 bits to identify one of 12,720 port pairs along with one additional bit to indicate whether the connection between the port pairs is to be made or broken. Since the command conveyed on the PARALLEL bus must identify the two 2-bit Cx values (one for each of the two ports), the command could use a total of 18 bits in order to tell control interface circuit 16 to make or break a connection between two particular ports and to set the Cx field inputs to the two ports.

Detailed Description Text (12):
However in the preferred embodiment of the invention, the command is reduced to eight bits to limit the size of the PARALLEL bus that conveys it. Of course an 8-bit command can have only one of 256 different values, and is therefore not large enough to select any one of the large number make/break/mode select combinations that would be needed to make full use of the routing and port mode capability of switch 10. But in accordance with the invention, the additional programming data supplied to control interface circuit 16 via the JTAG bus tells it how to set the value of data in SRAM 14 in response to each possible value of the 8-bit command arriving on the PARALLEL bus. As long as a data routing application employing switch 10 requires no more than 256 different switch control combinations, the 8-bit command width limitation does not prevent switch 10 from carrying out the application's data routing needs.

Detailed Description Text (13):
FIG. 2 illustrates control interface circuit 16 in more detailed block diagram form. The JTAG bus includes three lines TDI, TCK, and TMS. The TDI line carries data in serial form and the TCK line carries a clock signal. The host computer pulses the TMS line to indicate that it is about to transmit an instruction code on the TDI line. To write data into SRAM 14 of FIG. 1, a host computer first sends a pulse on the TMS line to tell a state machine 20 that an instruction is to follow on the TDI line. The host computer then sends a short serial "SRAM load" code to state machine 20 via the TDI line using the TCK line to clock each bit. State machine 20, programmed to respond to that code and clocked by a high frequency clock signal CLK, sends an input enable signal E1 to a serial-in/parallel-out shift register 22. Thereafter, on each pulse of the TCK clock signal from the host computer, shift register 22 shifts in a bit of a data sequence the host computer sends to shift register 22 via the TDI line. The data sequence includes an 8-bit ADDR field referencing the address of SRAM 14 (FIG. 1) at which data is to be written, an 8-bit PORT field Sx and a 2-bit port mode control field Cx. State machine 20 counts pulses of the TCK signal and when it determines that all bits of the sequence have been stored in shift register 22, state machine 20 turns off the E1 enable signal. A decoder 24 decodes the 8-bit PORT field in shift register 22 to produce the 160-bit Sx field. Decoder 24 sets all bits but one bit of the Sx field low when a connection is to be established between a switch port corresponding to the SRAM address and another port identified by the PORT field. The value of the PORT field tells decoder 24 which bit (0 to 159) of the Sx field to set high. When the PORT field has a value of 160, decoder 24 sets all bits of the Sx field low to that the port corresponding to the SRAM address is disconnected from all other ports. The 160 Sx output data bits of decoder 24 and the two Cx data bits stored in shift register 22 are placed on the DATA line inputs to SRAM 14 of FIG. 1. A decoder 26 decodes the 8-bit ADDR field stored in shift register 22 to produce a

160-bit output ADDR' field having one bit set high. A tristate buffer 28, when enabled, links the ADDR' field to the 160-line WORD select bus input to SRAM 14. After state machine 20 turns off the E1 signal, it pulses a signal E2 briefly enabling tristate buffer 28 to send a pulse on one of the WORD lines, thereby writing the Cx and Sx data to the SRAM 14 address identified by the ADDR field. The host computer repeats this process 160 times when initially programming switch 10 to load data into all 160 addresses of SRAM 14. Thereafter the host computer can repeat the process whenever it wants to change the data at any address of SRAM 14.

Detailed Description Text (14):
Control interface circuit 16 of FIG. 2 also includes a parallel bus interface circuit 30 that allows the host computer to use the PARALLEL bus to quickly write data to SRAM 14. Normally a set of tristate buffers 32 deliver the data stored in shift register 22 to decoders 24 and 26 and to the Cx lines of the DATA bus. However when the host computer sends a command via the PARALLEL bus, interface circuit 30 tristates buffers 32 and enables another set of tristate buffers 34 to couple its own Cx, PORT, and ADDR output fields to the Cx lines of the DATA bus and to decoders 24 and 26. Each command arriving on the PARALLEL bus tells interface circuit 30 to make or break a connection by writing data to the two SRAM 14 addresses corresponding to the two ports to be connected or disconnected. After receiving a command on the PARALLEL bus, interface circuit 30 generates the Cx, PORT and ADDR data for the first SRAM write operation and then pulses the E2 signal to enable tristate buffer 28, thereby writing the data to SRAM 14. Interface circuit 30 then produces the Cx, PORT and ADDR data for the second SRAM write operation and again pulses the E2 signal to initiate the second SRAM write operation.

Detailed Description Text (15):
FIG. 3 illustrates parallel bus interface circuit 30 of FIG. 2 in more detailed block diagram form. A command arriving on the PARALLEL bus includes an 8-bit ADDRESS field applied to a random access memory (RAM) 36 and a READ bit supplied to a state machine 38. At each of its 256 addressable storage locations RAM 36 stores 8-bit ADDR1 and ADDR2 fields, an 8-bit PORT1 field and 2-bit Cx1 and CX2 fields. When the host sends a command via the PARALLEL bus, RAM 36 reads out data stored at the address indicated the ADDRESS field. The read-out data, along with a hard-wired PORT2 field having a value of 160, are supplied to a multiplexer 40 controlled by an output signal E3 produced by state machine 38. The READ bit in the command conveyed on the PARALLEL bus tells state machine 38 to set multiplexer 40 so that it initially selects and provides the read out ADDR1, PORT1 and CX1 fields as the ADDR, PORT and CX field outputs of interface circuit 30. State machine 30 also sets the SEL signal so that buffers 34 of FIG. 2 forward that data to decoders 24 and 26 and the CX lines of the DATA bus. State machine 38 then pulses the E2 control input to buffer 28 to write data to the a first address of SRAM 14. State machine 38 then switches multiplexer 40 so that it selects its input ADDR2, CX2 and PORT2 fields as the sources of its output ADDR, CX and PORT fields, and then pulses the E2 once again to write data to the second SRAM 14 address.

Detailed Description Text (16):
The host computer may use the JTAG bus to change the data stored in any location of RAM 36. This changes how any particular ADDRESS value the host computer supplies on the PARALLEL bus alters connections between switch ports P0-P159 and sets their operating modes. The TMS, TDI and TCK lines of the JTAG bus provide inputs to state machine 38. When the host computer pulses the TMS line and sends a code over the TDI line indicating that data is to be loaded into RAM 36, state machine 38 asserts a signal E4 to enable a serial-in/parallel-out shift register 42. Thereafter the host computer sends a data sequence over the TDI line to shift register 42 using the TCK signal to shift each bit into register 42. The data sequence includes data to be written to RAM 36 and the address to which it is to be written. State machine 38 counts pulses of the TCK signal to determine when the data and address fields have been loaded into register 42. At that point state machine 38 deasserts the E4

signal and pulses a WRITE signal input to RAM 36 causing it to store the data field output of register 42 at the indicated address.

Detailed Description Text (17):
FIG. 4 illustrates port P0 of FIG. 1 in more detailed block diagram form. Ports P1-P159 are similar. Port P0 can operate in any one of several operating modes. The current 2-bit C0 field output of SRAM 14 of FIG. 1 read addresses a RAM 50 having four addressable storage locations. Data stored at currently addressed RAM 50 location selects the operating mode of port P0. Thus the 2-bit C0 field can select any one of four port operating modes. A host computer may use the JTAG bus to write data to each address of RAM 50 thereby determining which four of the many possible operating modes are available for selection by the incoming C0 field. To write data to an address of RAM 50 a host computer sends a TMS signal pulse to a state machine 52 and then sends a code to state machine 52 via the TDI line telling it that data is to be written to the RAM 50 of port P0. (The state machine 52 in each port P0-P159 responds to a different code so that the host may independently write data to the RAM 50 in each port.) State machine 52 responds to the code by asserting an enable signal E5 input of a serial-in/parallel-out shift register 54. The host then loads a data sequence into register 54 including data to be written to RAM 50 and the RAM address to receive it. State machine 52 counts pulses of the TCK signal that clocks the data sequence into shift register 54 and, when the data sequence is fully loaded into register 54, state machine 52 turns off the E5 signal and sends a WRITE pulse causing RAM 50 to store the data at the indicated address.

Detailed Description Text (29):
Several crosspoint switches can be interconnected in various ways to provide a larger signal routing system. For example, as illustrated in FIG. 5, two ports 72 of each of a set of N crosspoint switches 10A-10N is connected to a parallel bus 74. This allows devices connected to other ports 76 of each switch 10A-10N to communicate with each other even though they may not be connected to the same crosspoint switch. One port 72 of each switch 10A-10N is set to operate in a unidirectional input mode while the other port 72 of all switches 10A-10N is set to operate in a unidirectional, tristate output mode. One could alternatively set all ports 72 in bidirectional operating modes.

CLAIMS:

3. The crosspoint switch in accordance with claim 1 further comprising: a bus for conveying a command referencing a pair of said switch ports, said pair of switch ports consisting of a first switch port and a second switch port, wherein said command also references one of said plurality of operating modes to which said first switch port is to be set; and memory controller means connected to said bus for receiving and responding to said command by concurrently writing first routing control data and first mode control data to a first storage location of said memory means corresponding to said first switch port.

5. The crosspoint switch in accordance with claim 3 wherein said command consists of a plurality of bits and wherein said bus is a parallel bus that concurrently conveys all bits of said command.

6. The crosspoint switch in accordance with claim 1 further comprising: a bus for conveying a command; memory controller means for receiving and decoding said command to generate a first address, first routing data and first mode control data, and for writing said first routing data and said first mode control data to said first addressable storage location of said memory means.

First Hit Fwd Refs

Generate Collection Print

L4: Entry 4 of 33 File: USPT Jan 14, 2003

US-PAT-NO: 6507581
DOCUMENT-IDENTIFIER: US 6507581 B1

TITLE: Dynamic port mode selection for crosspoint switch

DATE-ISSUED: January 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sgammato; Frank J.	San Jose	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Fairchild Semiconductor Corporation	South Portland	MA			02

APPL-NO: 09/ 097177 [PALM]
DATE FILED: June 12, 1998

INT-CL: [07] H04 Q 1/00

US-CL-ISSUED: 370/381; 370/423, 340/2.26, 710/100, 326/38
US-CL-CURRENT: 370/381; 326/38, 340/2.26, 370/423, 710/100

FIELD-OF-SEARCH: 370/381, 370/423, 370/392, 370/429, 340/2.26, 340/2.2, 340/2.21, 326/38, 326/41, 326/82, 326/86, 326/46, 710/100

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5282271	January 1994	Hsieh et al.	340/2.26
☐	5428750	June 1995	Hsieh et al.	710/100
☐	5465056	November 1995	Hsieh et al.	326/38
☐	5710550	January 1998	Hsieh et al.	370/423
☐	5734334	March 1998	Hsieh et al.	370/392
☐	6097211	August 2000	Couts-Martin et al.	326/46
☐	6259271	July 2001	Couts-Martin et al.	326/41

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ART-UNIT: 2635

PRIMARY-EXAMINER: Zimmerman; Brian

ATTY-AGENT-FIRM: Bedell; Daniel J. Smith-Hill and Bedell

ABSTRACT:

A crosspoint switch includes a large number of ports and a separate pass transistor linking each possible pair of ports. When a pass transistor is turned on or off, it makes or breaks a signal path between the pair of ports it links. Each port can process signals passing through the port in any one of several operating modes, with a current operating mode being selected by input mode control data. The crosspoint switch also includes a random access memory (RAM) having a separate addressable storage location corresponding to each port. Each RAM storage location stores routing data for controlling the pass transistors connected to a corresponding port and also stores mode control data controlling the mode of the corresponding port. A memory controller responds to a parallel command from a host computer by concurrently writing routing and mode control data to two storage location of the RAM, thereby quickly making and/or breaking a signal path between two ports and selecting the operating mode of both ports.

14 Claims, 6 Drawing figures

First Hit Fwd Refs

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L4: Entry 8 of 33 File: USPT Feb 27, 2001

US-PAT-NO: 6195719
DOCUMENT-IDENTIFIER: US 6195719 B1

TITLE: Bus system for use with information processing apparatus

DATE-ISSUED: February 27, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Okazawa; Koichi	Tokyo			JP
Kimura; Koichi	Yokohama			JP
Kawaguchi; Hitoshi	Yokohama			JP
Aburano; Ichiharu	Hitachi			JP
Kobayashi; Kazushi	Ebina			JP
Mochida; Tetsuya	Yokohama			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 09/ 518696 [PALM]
DATE FILED: March 3, 2000

PARENT-CASE:
This is a continuation application of U.S. Ser. No. 09/375,356, filed Aug. 17, 1999 U.S. Pat. No. 6,098,136; which is a continuation application of U.S. Ser. No. 09/276,968 filed on Mar. 26, 1999 U.S. Pat. No. 6,006,302; which is a continuation application of U.S. Ser. No. 09/143,985, filed Aug. 31, 1998 U.S. Pat. No. 5,935,231; which is a continuation application of U.S. Ser. No. 08/959,913, filed Oct. 29, 1997 U.S. Pat. No. 5,889,971; which is a continuation application of U.S. Ser. No. 08/601,993, filed Feb. 15, 1996, now U.S. Pat. No. 5,751,976; which is a continuation application of U.S. Ser. No. 08/449,088, filed May 24, 1995, now U.S. Pat. No. 5,668,956; which is a continuation application of U.S. Ser. No. 08/311,893, filed Sep. 26, 1994, now U.S. Pat. No. 5,483,642; which is a continuation application of U.S. Ser. No. 07/705,701, filed May 23, 1991, now abandoned.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2-144301	June 4, 1990
JP	3-105536	May 10, 1991

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 710/126; 710/129
US-CL-CURRENT: 710/311; 710/313

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FIELD-OF-SEARCH: 710/126, 710/129, 710/128

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4016546	April 1977	Bennett et al.	
☐	4439829	March 1984	Tsiang	
☐	4665483	May 1987	Ciacci et al.	
☐	4695944	September 1987	Zandveld et al.	
☐	4700348	October 1987	Ise et al.	
☐	4780813	October 1988	Gierety	
☐	4851990	July 1989	Johnson et al.	
☐	4945267	July 1990	Galbraith	
☐	4945540	July 1990	Kaneko	
☐	4982321	January 1991	Pantry et al.	
☐	5003465	March 1991	Chisholm et al.	
☐	5274795	December 1993	Vachon	
☐	5359715	October 1994	Heil et al.	
☐	5506973	April 1996	Okazawa et al.	
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Baran, "EISA Arrives", BYTE, vol. 14, No. 12, Nov. 1989, pp. 93-98.
"The Surging RISC", Nikkei Electronics, No. 474, May 29, 1989, pp. 106-119.

ART-UNIT: 271

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PRIMARY-EXAMINER: Auve; Glenn A.

ATTY-AGENT-FIRM: Mattingly, Stanger & Malur

ABSTRACT:

A processor bus linked with at least a processor, a memory bus linked with a main memory, and a system bus linked with at least an input/output device are connected to a three-way connection control system. The control system includes a bus-memory connection controller connected to address buses and controL buses respectively of the processor, memory, and system buses to transfer address and control signals therebetween. The control system further includes a data path switch connected to data buses respectively of the processor, memory, and system buses to transfer data via the data buses therebetween depending on the data path control signal.

30 Claims, 19 Drawing figures

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L4: Entry 20 of 33 File: USPT Sep 16, 1997

US-PAT-NO: 5668956
DOCUMENT-IDENTIFIER: US 5668956 A
**** See image for Certificate of Correction ****

TITLE: Bus system for use with information processing apparatus

DATE-ISSUED: September 16, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Okazawa; Koichi	Tokyo			JP
Kimura; Koichi	Yokohama			JP
Kawaguchi; Hitoshi	Yokohama			JP
Aburano; Ichiharu	Hitachi			JP
Kobayashi; Kazushi	Ebina			JP
Mochida; Tetsuya	Yokohama			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 08/ 449088 [PALM]
DATE FILED: May 24, 1995

PARENT-CASE:
This application is a continuation application of U.S. Ser. No. 08/311,893, filed Sep. 26, 1994 U.S. Pat. No. 5,483,642; which is a continuation application of U.S. Ser. No. 07/705,701, filed May 23, 1991, now abandoned .

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	2-144301	June 4, 1990
JP	3-105536	May 10, 1991

INT-CL: [06] G06 F 13/14

US-CL-ISSUED: 395/306; 395/309
US-CL-CURRENT: 710/306; 396/309

FIELD-OF-SEARCH: 395/325, 395/309, 395/311, 395/281, 395/306

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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☐	4665483	May 1987	Ciacci et al.	395/325
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☐	4780813	October 1988	Gerety et al.	395/866
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☐	4945267	July 1990	Galbraith	307/571
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Baran, "EISA Arrives", BYTE, V. 14, No. 12, Nov. 1989, pp. 93-98.
"The Surging RISC", Nikkei Electronics, No. 474, May, 29, 1989, pp. 106-119 .

ART-UNIT: 235

PRIMARY-EXAMINER: Auve; Glenn A.

ABSTRACT:

A processor bus linked with at least a processor, a memory bus linked with a main memory, and a system bus linked with at least an input/output device are connected to a three-way connection control system. The control system includes a bus-memory connection controller connected to address buses and control buses respectively of the processor, memory, and system buses to transfer address and control signals therebetween. The control system further includes a data path switch connected to data buses respectively of the processor, memory, and system buses to transfer data via the data buses therebetween depending on the data path control signal.

7 Claims, 19 Drawing figures

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US006662282B2

(12) **United States Patent**
Cochran

(10) **Patent No.: US 6,662,282 B2**
(45) **Date of Patent: Dec. 9, 2003**

(54) **UNIFIED DATA SETS DISTRIBUTED OVER MULTIPLE I/O-DEVICE ARRAYS**

(75) Inventor: **Robert A. Cochran**, Rocklin, CA (US)

(73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 171 days.

(21) Appl. No.: **09/837,311**

(22) Filed: **Apr. 17, 2001**

(65) **Prior Publication Data**

US 2002/0152362 A1 Oct. 17, 2002

(51) **Int. Cl.**[7] **G06F 12/00**
(52) **U.S. Cl.** **711/162; 711/111**
(58) **Field of Search** 711/162, 112, 711/111, 114; 714/6

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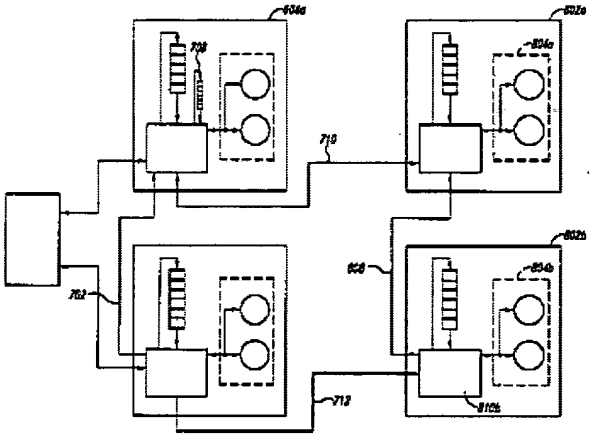
Primary Examiner—Kimberly McLean-Mayo

(57) **ABSTRACT**

A hardware configuration and methodology for serializing or partially serializing WRITE requests directed to a unified data set are subsequently distributed to one or more remote arrays containing a corresponding mirror unified data set. For each unified data set, one of the local disk arrays over which the unified data set is distributed is selected as a supervisor disk array, and a unified sequence number component is included within that supervisor disk array. WRITE requests generated by a local array to mirror unified data set data to a mirror unified data set must be associated with a unified sequence number, and the WRITE requests are therefore serialized or partially serialized by the unified sequence number component. Additional direct communications links are provided between the local arrays over which a unified data set is distributed both to facilitate WRITE-request serialization and to provide a redundant communications paths for added reliability.

18 Claims, 15 Drawing Sheets



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[45] Date of Patent: Jul. 6, 1999

[54] **PROGRAMMABLE CIRCUIT ASSEMBLY AND METHODS FOR HIGH BANDWIDTH DATA PROCESSING**

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[58] Field of Search 711/100, 103, 711/104, 105, 109, 101; 326/39, 41; 340/825.83; 365/51, 63, 189.08

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Attorney, Agent, or Firm—Jerome D. Jackson

[57] **ABSTRACT**

A programmable circuit assembly and methods for high bandwidth data processing. The assembly includes an array of in-circuit programmable logic packages interconnected with an array of memory packages, allowing for elastic buffering of data in a variety of directions. Each programmable package includes package leads, a memory, and output drivers. Each output driver is connected to a respective package lead, which is configured to generate a logic function defined by programming data stored in the memory. A method includes storing programming data for operating the assembly to send signals on different paths between a programmable package and a memory package.

18 Claims, 19 Drawing Sheets